

Appl. No. 09/115,444  
Amdt. Dated November 26, 2003  
Reply to Office Action dated August 13, 2003

### **Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1. (previously presented) An integrated circuit package comprising:  
a multilayer substrate comprising a top layer having a top surface and a bottom layer having a bottom surface opposite said top surface, said top and said bottom layers having a plurality of overlapping peripheral openings, wherein said openings are larger in said top layer than in said bottom layer such that a portion of a top surface of said bottom layer is exposed;  
a plurality of routing strips on said top surface of said bottom layer, wherein at least one of said routing strips is on said exposed portion of said top surface of said bottom layer;  
a chip adhered to said bottom surface of said bottom layer of said substrate;  
a plurality of electrical conductors physically attached to said chip and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate;  
a plurality of pads disposed on said top surface of said top layer of said substrate generally centralized within said peripheral openings of said substrate; and  
potting material filling said peripheral openings.

Claim 2. (cancelled)

Claim 3. (previously presented) The integrated circuit package as recited in claim 1 wherein at least one of said pads disposed on said top surface of said top layer of said substrate is electrically connected with said at least one of said routing strips.

Claim 4. (previously presented) The integrated circuit package as recited in claim 3 wherein at least one of said pads disposed on said top surface of said top layer of said substrate is electrically connected with said at least one of said routing strips with a via through said top layer of said substrate.

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Claim 5. (original) The integrated circuit package as recited in claim 1 further comprising at least one solder ball disposed on one of said pads.

Claim 6. (previously presented) The integrated circuit package as recited in claim 1 further comprising a plurality of solder balls disposed on said pads.

Claim 7. (original) The integrated circuit package as recited in claim 1 wherein said potting material adheres said chip to said substrate.

Claim 8. (previously presented) An integrated circuit package comprising:  
a multilayer substrate comprising a top layer having a top surface and a bottom layer having a bottom surface opposite said top surface, said top and said bottom layers having a plurality of overlapping peripheral openings, wherein said openings are larger in said top layer than in said bottom layer such that a portion of a top surface of said bottom layer is exposed;  
a plurality of routing strips on said top surface of said bottom layer, wherein at least one of said routing strips is on said exposed portion of said top surface of said bottom layer;  
a plurality of pads disposed centrally on said top surface, at least one of said pads being electrically connected with said at least one of said routing strips;  
potting material filling said plurality of peripheral openings;  
a chip having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate; and  
wire bonding electrically connecting said chip to said substrate between at least one of said bonding pads and said at least one of said routing strips on said exposed portion of said top surface of said bottom layer.

Claim 9. (original) The integrated circuit package as recited in claim 8 further comprising at least one solder ball disposed on one of said pads.

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Claim 10. (original) The integrated circuit package as recited in claim 9 wherein said at least one solder ball is between about 8 and 20 mils in diameter.

Claim 11. (previously presented) The integrated circuit package as recited in claim 8 further comprising a plurality of solder balls disposed on said pads.

Claim 12. (original) The integrated circuit package as recited in claim 8 wherein said chip has a thickness between about 10 and 20 mils.

Claim 13. (original) The integrated circuit package as recited in claim 8 wherein said substrate has a thickness of between about 8 and 28 mils.

Claim 14. (original) The integrated circuit package as recited in claim 8 wherein said substrate has first and second layers and wherein said first layer has a thickness of about 12 mils and said second layer has a thickness of about 8 mils.

Claim 15. (previously presented) The integrated circuit package as recited in claim 8 wherein said at least one of said pads being electrically connected with said at least one of said routing strips is connected by a via through said top layer of said substrate.

Claim 16. (previously presented) An integrated circuit package comprising:  
a substrate having a plurality of peripheral openings, first and second surfaces and an outline;  
a plurality of routing strips being integral with said substrate;  
a plurality of pads centrally disposed on said first surface at least one of said pads being electrically connected with said routing strips;  
a chip adhered to said second surface of said substrate, said chip having an outline that is substantially the same as said outline of said substrate and having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of

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bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate;

wire bonding electrically connecting said bonding pads to said routing strips;

vias connecting said routing strips to said pads;

potting material filling said peripheral openings and covering said wire bonding and said bonding pads; and

a plurality of solder balls centrally disposed on said pads disposed on said first surface of said substrate.

Claim 17. (original) The integrated circuit package as recited in claim 16 wherein said chip has a thickness between about 10 and 20 mils.

Claim 18. (original) The integrated circuit package as recited in claim 16 wherein said substrate has a thickness of between about 8 and 28 mils.

Claim 19. (original) The integrated circuit package as recited in claim 16 wherein said substrate has first and second layers and wherein said first layer has a thickness of about 12 mils and said second layer has a thickness of about 8 mils.

Claim 20. (previously presented) The integrated circuit package as recited in claim 19, wherein said peripheral openings in said second layer are larger than the peripheral openings in said first layer, such that a portion of a top surface of said first layer is exposed in each of said peripheral openings in said second layer.

Claim 21. (previously presented) The integrated circuit package of claim 1 wherein each of the plurality of conductors comprises a bonding pad.

Claim 22. (canceled)